EEE404/591 - Real-Time Digital Signal Processing

http://www.fulton.asu.edu/~karam/realdsp/

Introduction

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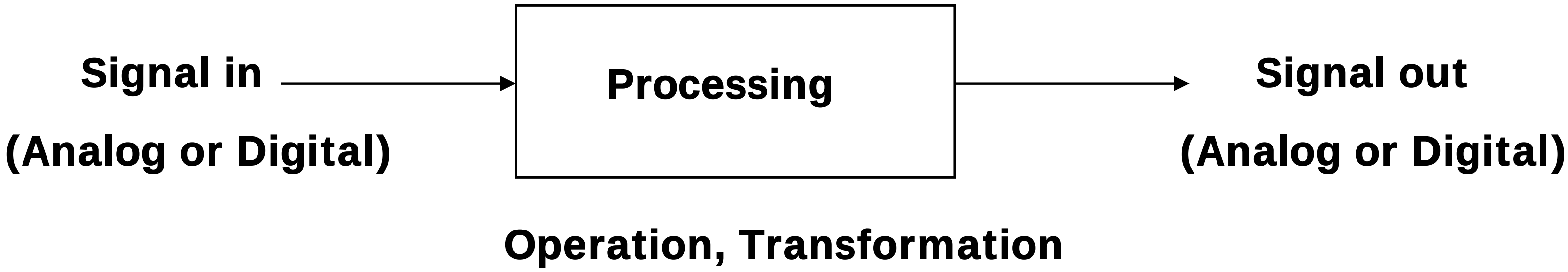
Arizona State University

What is Signal Processing?

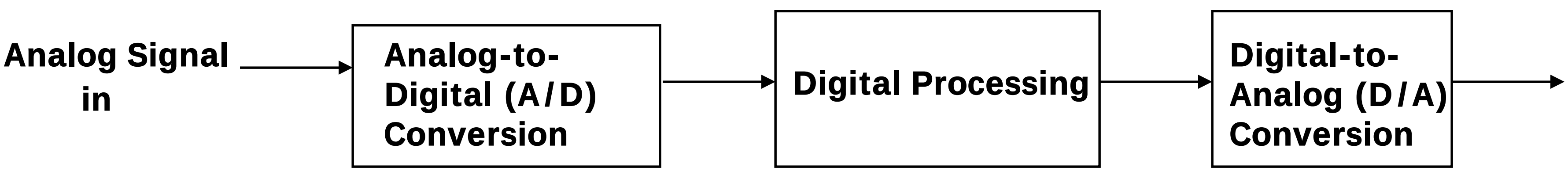


- Example of Signals:
  - Analog: Speech, Music, Photos, Video, radar, sonar, ...
  - Discrete-domain/Digital:
    - digitized speech, digitized music, digitized images, digitized video, digitized radar and sonar signals,...
    - stock market data, daily max temperature data, …

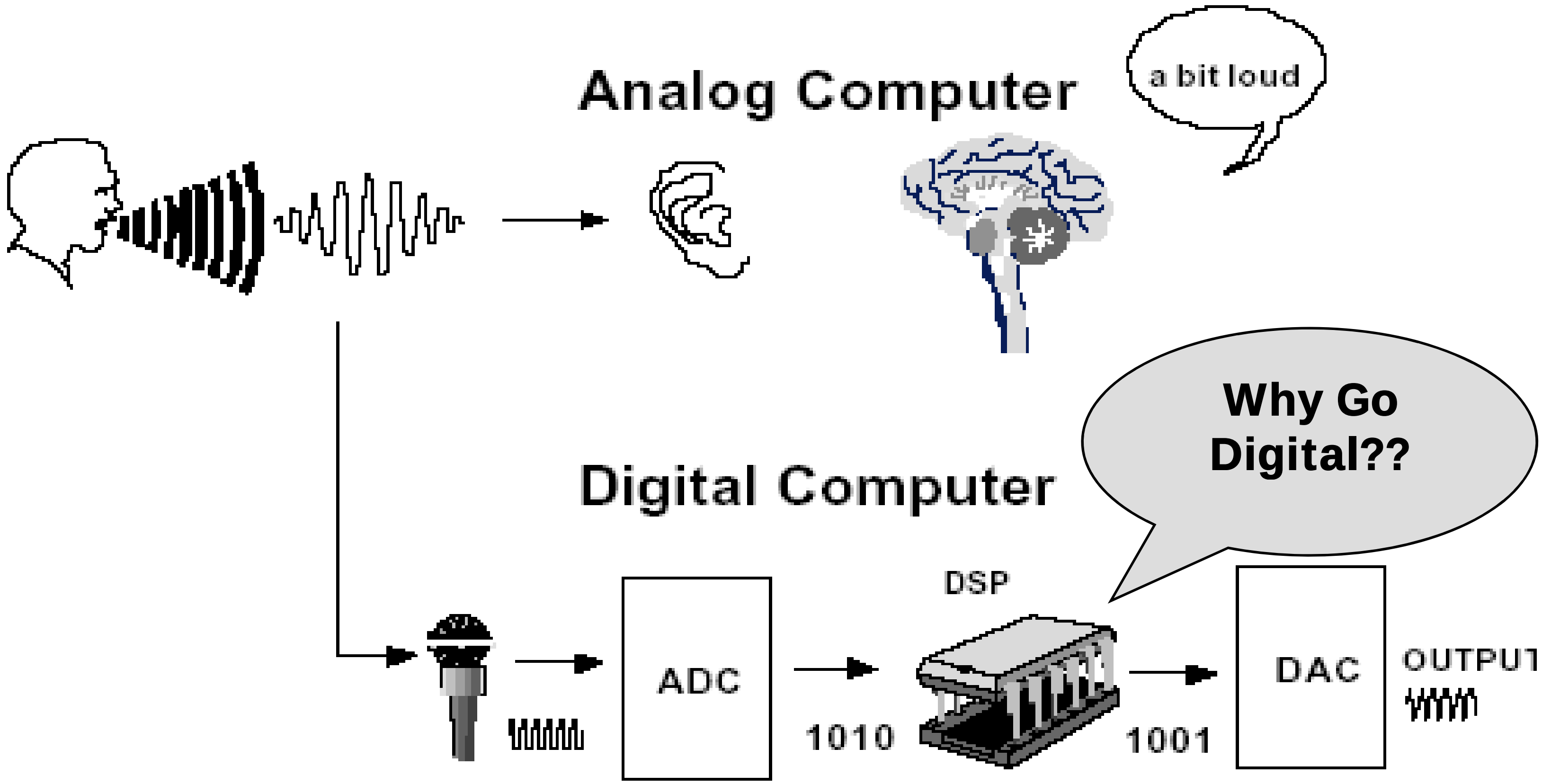
What is Digital Signal Processing?

Operation, Transformation performed on *digital* signals (using a computer or other special-purpose digital hardware)

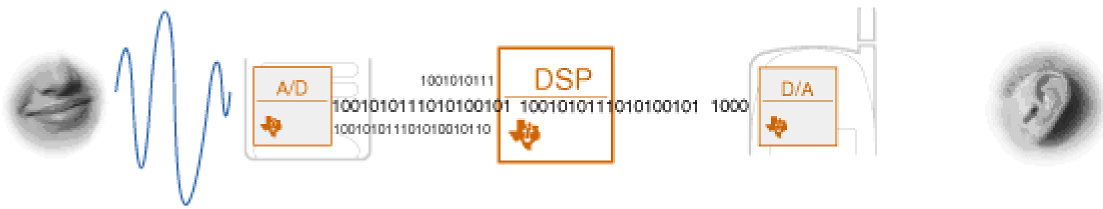
- But what about analog signals?



Signal Processing Examples



Typical Scenario



Step 1: **Analog sensor picking analog signal (i.e: microphone picking sound)**

Step 2: **Analog to Digital Converter**

Step 3: **DSP processes the digital signals (e.g., compression, noise suppression)**

Step 4: **Digital to analog converter to recover the analog signal**

What is Real-Time Digital Signal Processing?

Time-constrained Operation or Transformation performed on *digital* signals within a required period of time to maintain synchronization with occurring events.

- Example:
  - Processor clocked at 120 MHz and can perform 120MIPS
    - Sampling rate = 48KHz (Digital Audio Tape - DAT) number of instructions per sample = $(120 \times 10^6)/(48 \times 10^3) = 2500$.
    - Sampling rate = 8KHz (voice-band, telephony) number of instructions per sample = 15000.
    - Sampling rate = 75MHz (CIF 360x288 Video at 30 frames per second) number of instructions per sample = 1.6.

Real-Time Digital Signal Processing

- Constraints:
  - real-time DSP applications limited to cases where the required sampling rate is sufficiently lower than the processor's instruction rate
- Challenge:
  - Produce working code.
  - Produce sufficiently compact code to execute in real-time.
  - A sufficient number of instructions need to be performed between sample periods.

What is DSP?

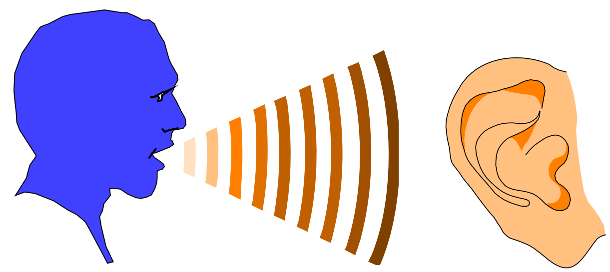
- DSP = Digital Signal Processing
  OR
  DSP = Digital Signal Processor?

- DSP used to denote both
  - meaning can be deduced from the context in which the term DSP is used.
- What is a Digital Signal Processor (DSP)?
  - Microprocessor specifically designed to perform fast DSP operations (e.g., Fast Fourier Transforms, inner products, Multiply & Accumulate)

Why Go Digital?

- Programmability
  - One hardware can perform several tasks.
  - Upgradeability and flexibility.
- Repeatability
  - Identical performance from unit to unit.
  - No drift in performance due to temperature or aging.
- Immune to noise
- Offers higher performance : CD players versus phonographic turntable

Signal Processing Applications



- Speech processing
  - Speech compression
  - Speech recognition
  - Speaker Identification, Verification
  - Speech synthesis
  - Speech enhancement, Echo cancellation
- Audio Processing
  - Compression
  - 3-D reproduction

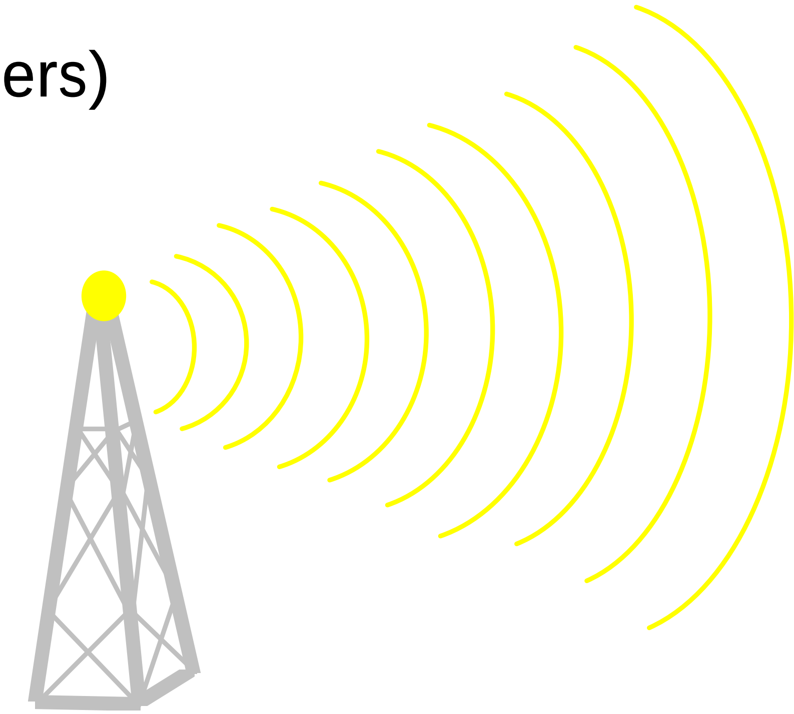
DSP Applications – Image Processing

- Image Processing
  - Image compression
  - Pattern recognition
  - Ghost cancellation
  - Noise reduction
  - Deblurring
  - Object tracking
  - Image fusion

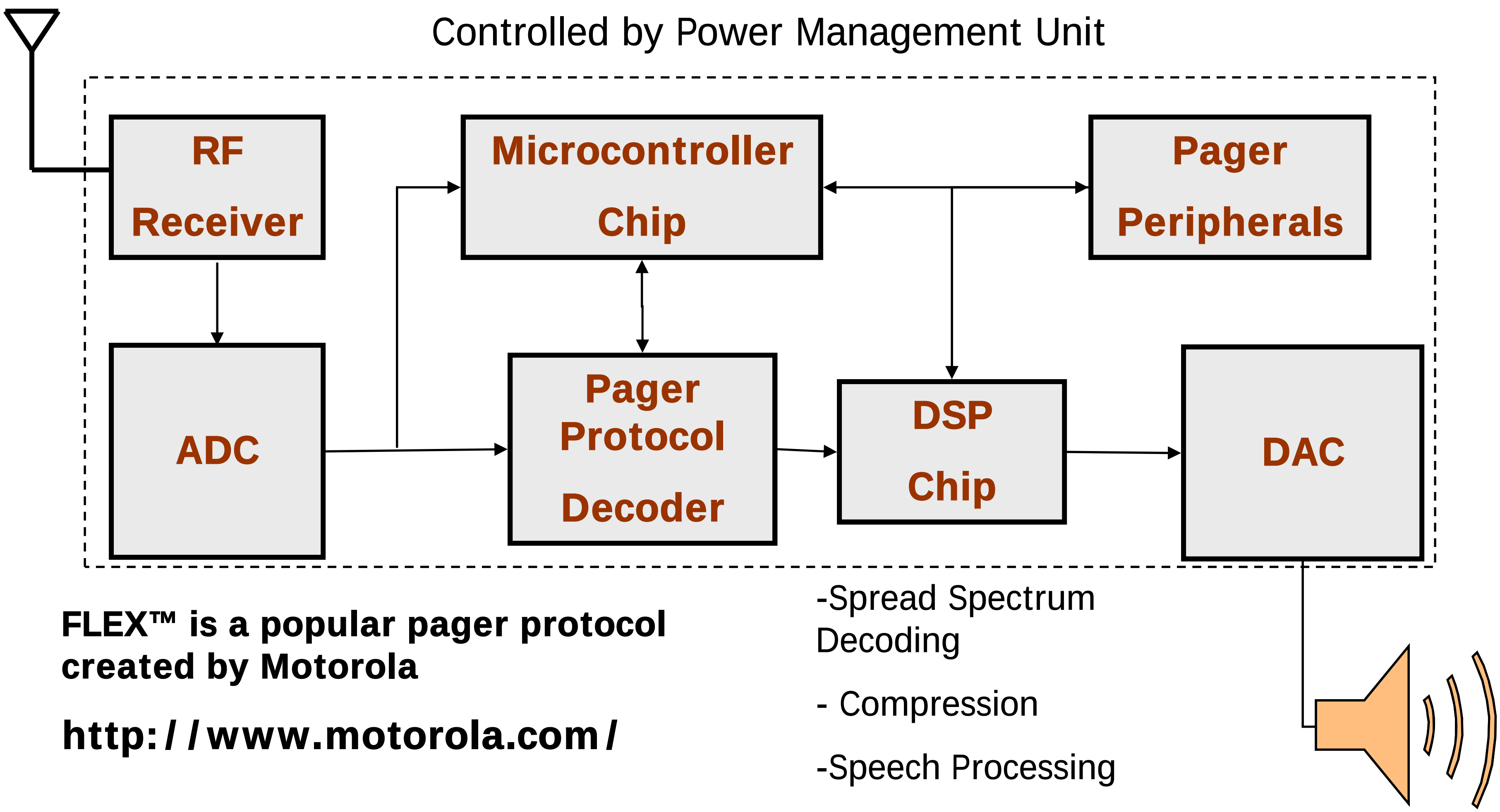
- Video Processing/compression, tracking…

DSP Applications Communications

- MODEM
  - correlators (matched filters)
  - echo cancellers
  - equalizers
- Cellular Telephony
  - speech compression
  - diversity combining
  - array processing
- Software Radio



DSP Targets: Pager



FLEX™ is a popular pager protocol created by Motorola

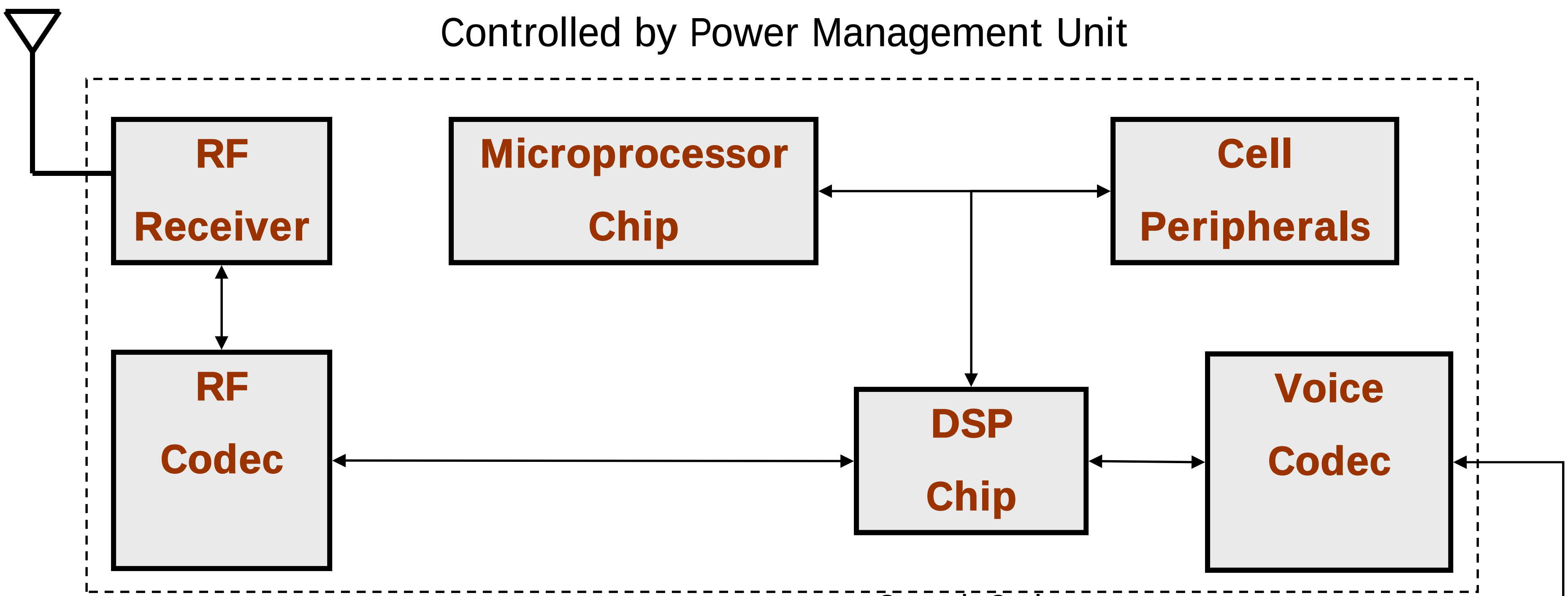
http://www.motorola.com/

-Spread Spectrum Decoding

- Compression

-Speech Processing

DSP Targets: Cell Phone



-Speech Coders

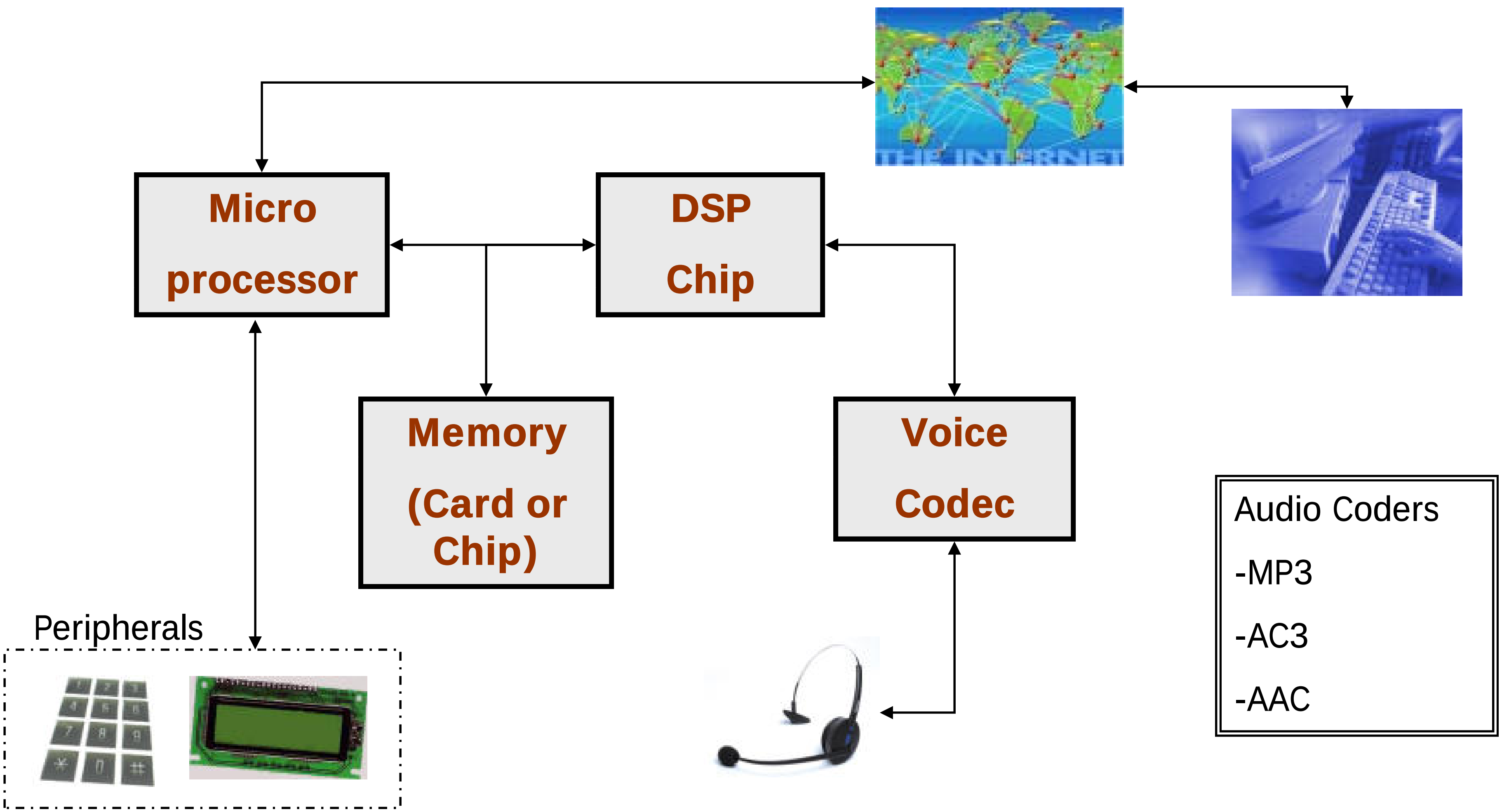
-Speech Recognition

- Equalizers

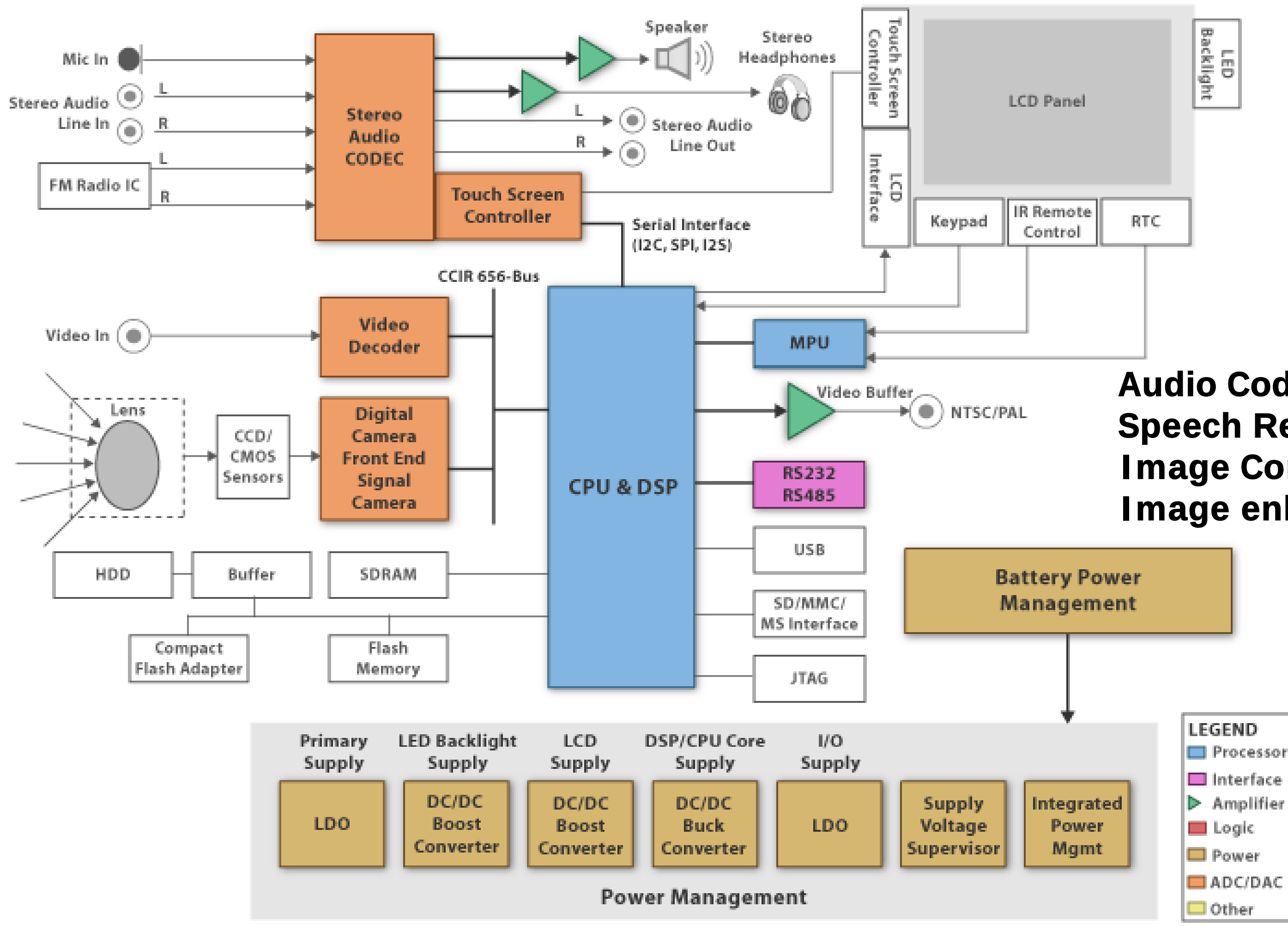
- Antenna noise cancellation

-Image enhancement techniques

DSP Targets: Voice Over IP



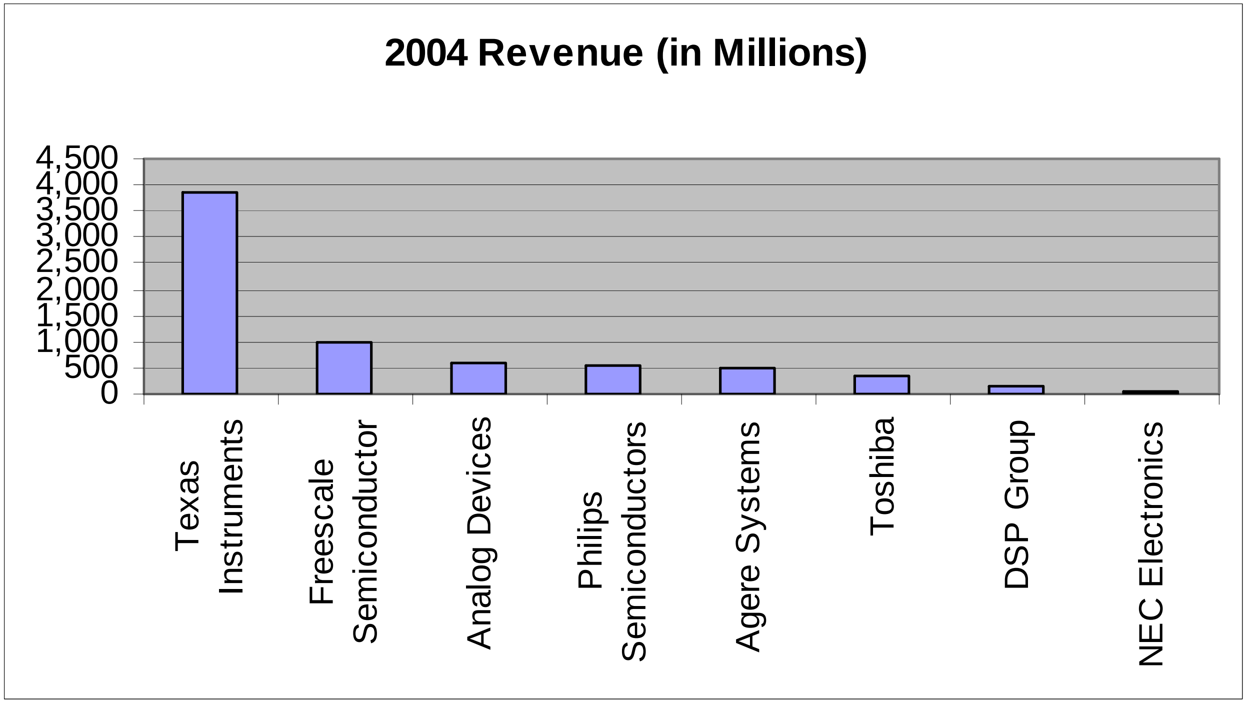
DSP Targets: PORTABLE MEDIA DEVICES



Audio Coding
Speech Recognition
Image Compression
Image enhancement

Web Link: http://focus.ti.com/vf/docs/blockdiagram.tsp?blockDiagramId=6046&appId=267

DSP Market – Ranking



Ranking:

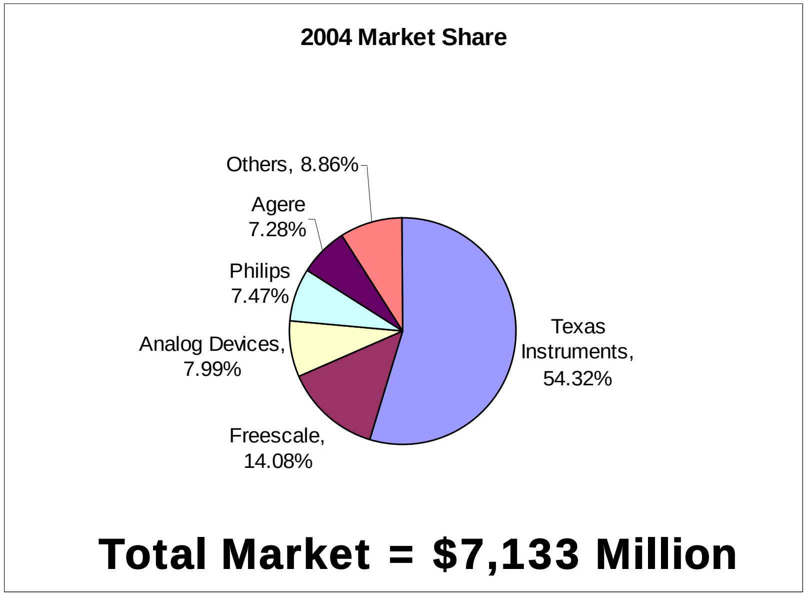
- **Texas Instruments**
- **Freescale Semiconductor**
- **Analog Devices**
- **Philips Semiconductors**
- **Agere Systems**
- **Toshiba**
- **DSP Group**
- **NEC Electronics**

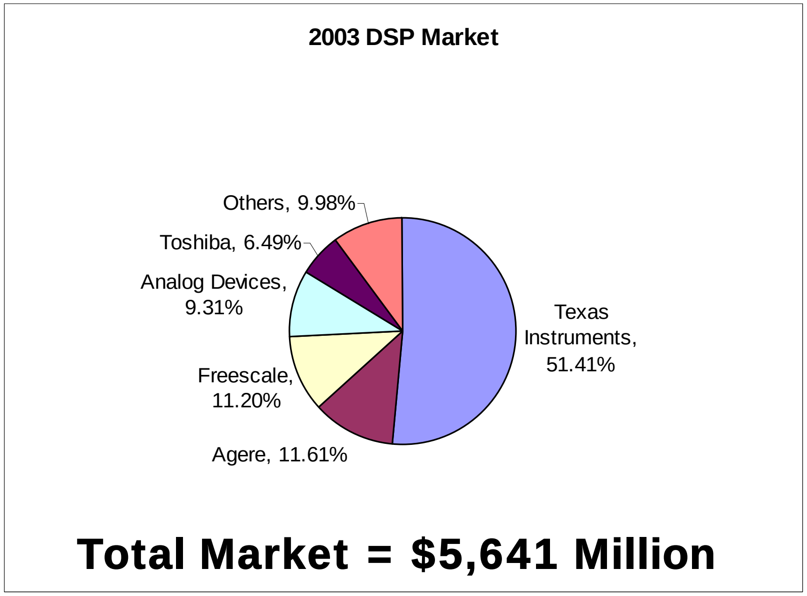
→ **Kits available in the lab are from TI and Freescale**

Ref: Reed Business Information

http://www.reed-electronics.com/moversandshakers/article/CA6277494.html

DSP Market – By Company





Ref: Forward Concepts

http://www.fwdconcepts.com/Pages/press42.htm

Portable Applications

- Embedded signal and image processing tasks are becoming more demanding
  - Wireless communications (e.g., 3G, UWB): higher data rates, more complex systems and air interfaces
  - Video processing (DTV, HDTV, Camcorders, 3DTV): compression, decompression, enhancement, superresolution, feature extraction
  - Still image processing: cameras, copiers, printers, image-based rendering
- High performance is required: 100s to 1000s of GOPs
- High efficiency: 100s of MOPS/mW (GOPS/mW), 10s GOPS/$
- Programmability: multiple modes, evolving standards, evolving features
- Move towards multi-core DSPs

What is Special about Signal Processing Applications?

- Large number of samples being continuously fed to the system (samples or blocks).
- Repetitive Operations:
  - The same operation being applied to different set of samples
  - Parallel processing
- Vector and Matrix Operations
- Real time operations

Example: Digital Filtering

- The two most common real-time digital filters are:
  - Finite Impulse Filter (FIR)
  - Infinite Impulse Filter (IIR)
- The basic FIR Filter equation is

$$y[n] = \sum h[k].x[n-k]$$

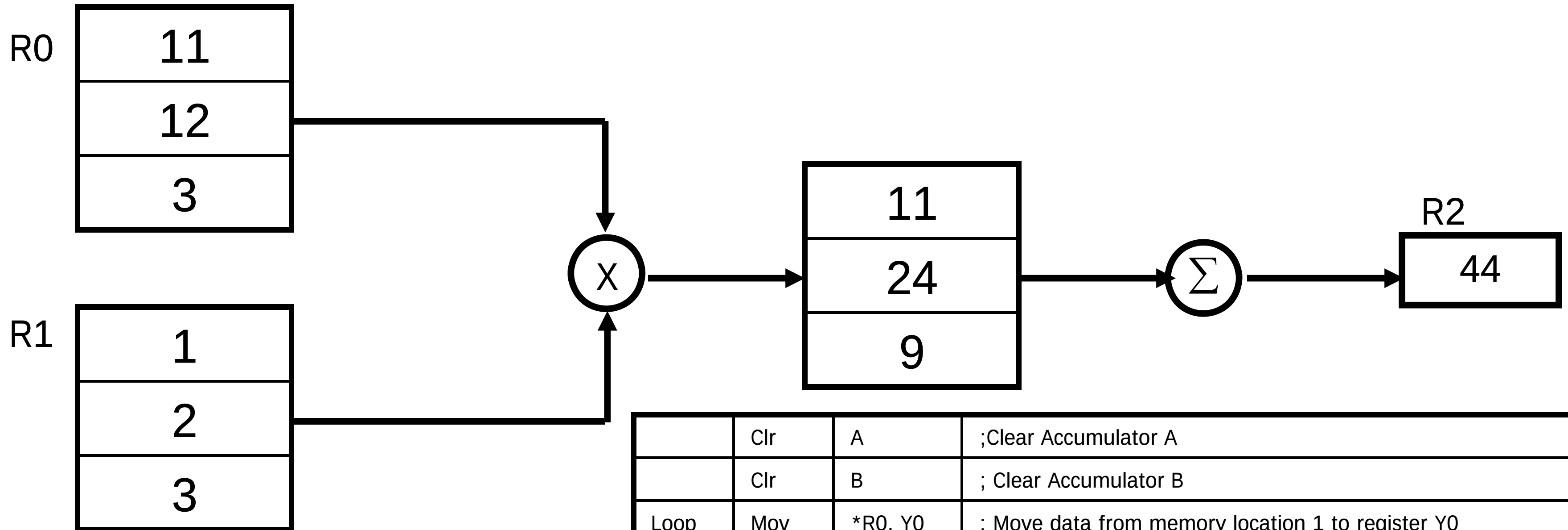
where h[k] is an array of constants

In C language

```
y[n]=0;
For (n=0; n<N;n++)
{
For (k = 0;k<N;k++)
//inner loop
            y[n] = y[n] + h[k]*x[n-k];}
```

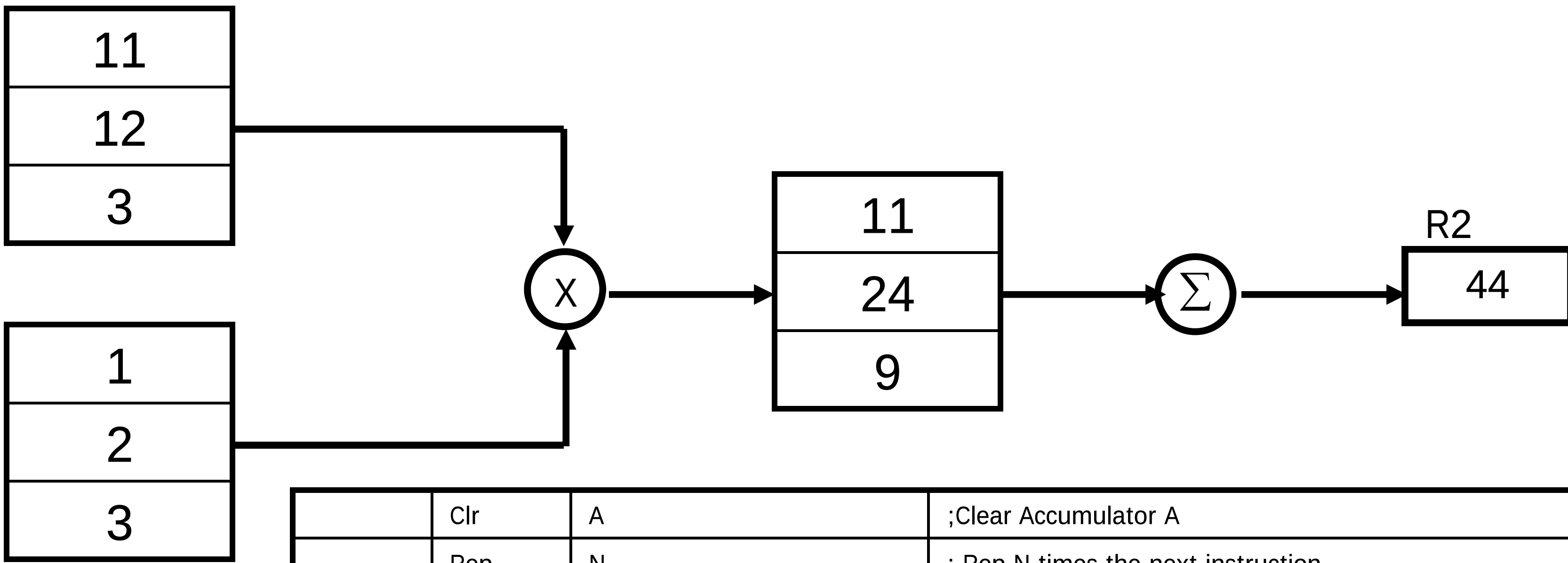
Only Multiply and Accumulate (MAC) is needed!

MAC using General Purpose Processor (GPP)



	Clr	A	;Clear Accumulator A
	Clr	B	; Clear Accumulator B
Loop	Mov	*R0, Y0	; Move data from memory location 1 to register Y0
	Mov	*R1,X0	; Move data from memory location 2 to register X0
	Mpy	X0,Y0,A	;X0*Y0 ->A
	Add	A,B	;A + B -> B
	Inc	R0	;R0 + 1 -> R0
	Inc	R1	;R1 + 1 -> R1
	Dec	N	;Dec N (initially equals to 3)
	Tst	N	;Test for the value
	Jnz	Loop	;Different than zero loop again
	Mov	B,*R2	;Move result to memory

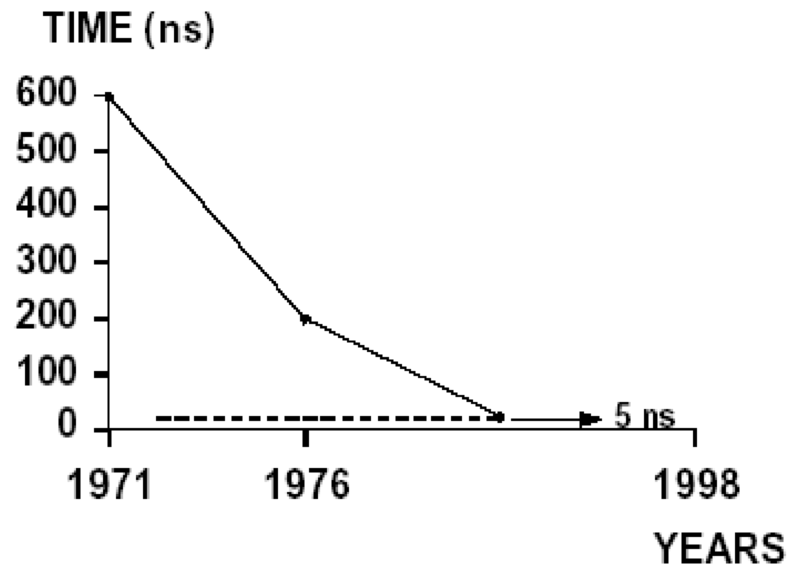
MAC using DSP



	Clr	A	;Clear Accumulator A
	Rep	N	; Rep N times the next instruction
	MAC	*(R0)+, *(R1)+, A	; Fetch the two memory locations pointed by R0 and R1, multiply them together and add the result to A, the final result is stored back in A
	Mov	A, *R2	; Move result to memory

Multiplier Design

- Early Attempts
  - AMI released S2811 in 1978
    - Math coprocessor
    - Never used in end product
    - Problem in fabrication technology
  - Intel released 2920 in 1979
    - ADC and DAC embedded
    - Harvard Architecture
    - Available Direct Addressing Only
    - No multiplier
- In early 1980s, single chip DSP with good performance started to appear (with MAC), and ever since multiplication times decreased
- First commercially successful DSP "DSP1" in 1980 from AT&T Bell Laboratories- Used mainly of in-house designs.
- TI first commercially successful DSP TMS32010 operating at 5 Mhz (200ns) in 1982. Sold for $120 per 100 pieces



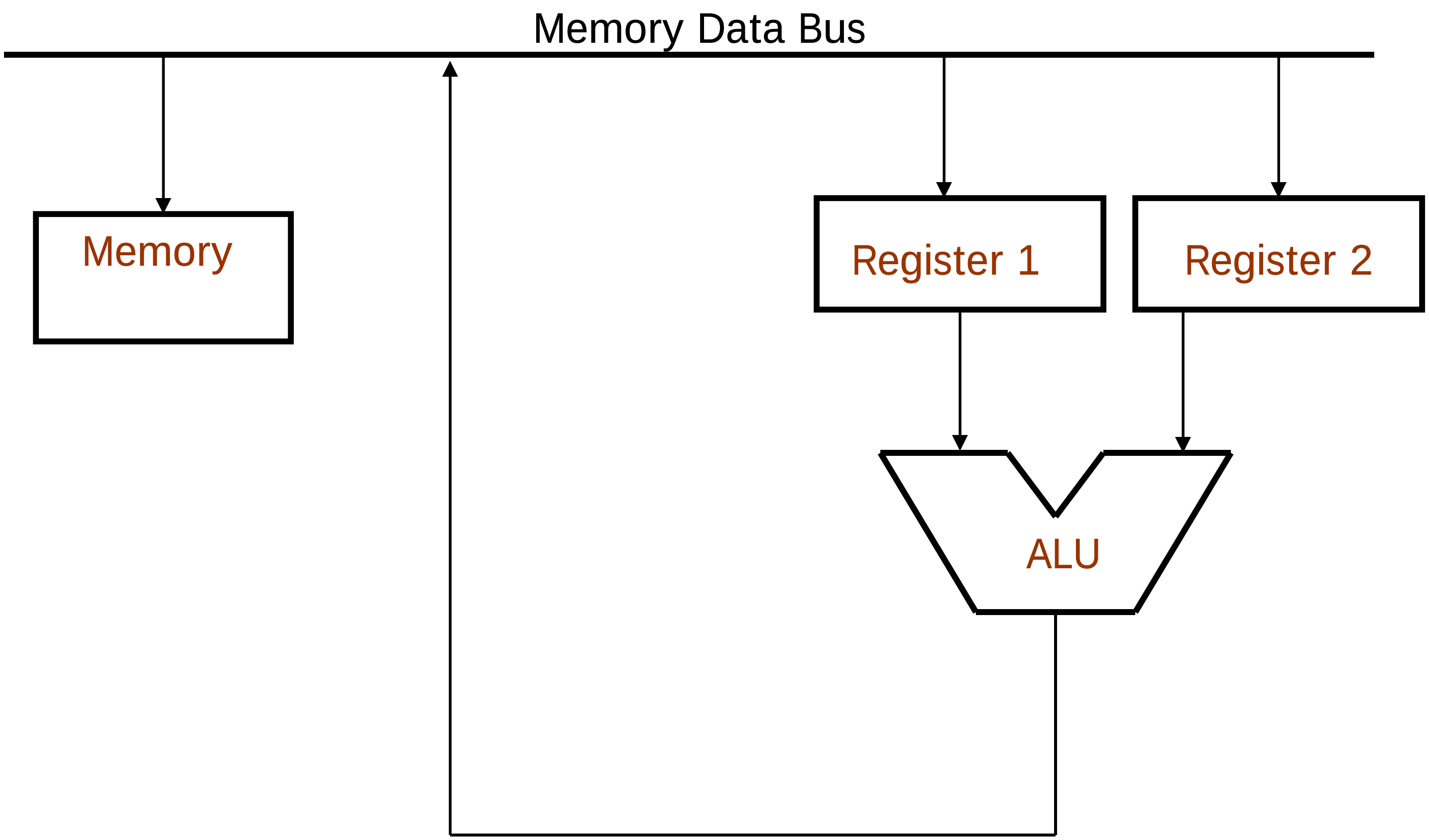
Ref: http://lsiwww.epfl.ch/LSI2001/teaching/webcourse/ch12/DSParch.htm

GPP Drawbacks

- More instructions/task
- Common Memory for data and program
  - Limited bus/memory bandwidth

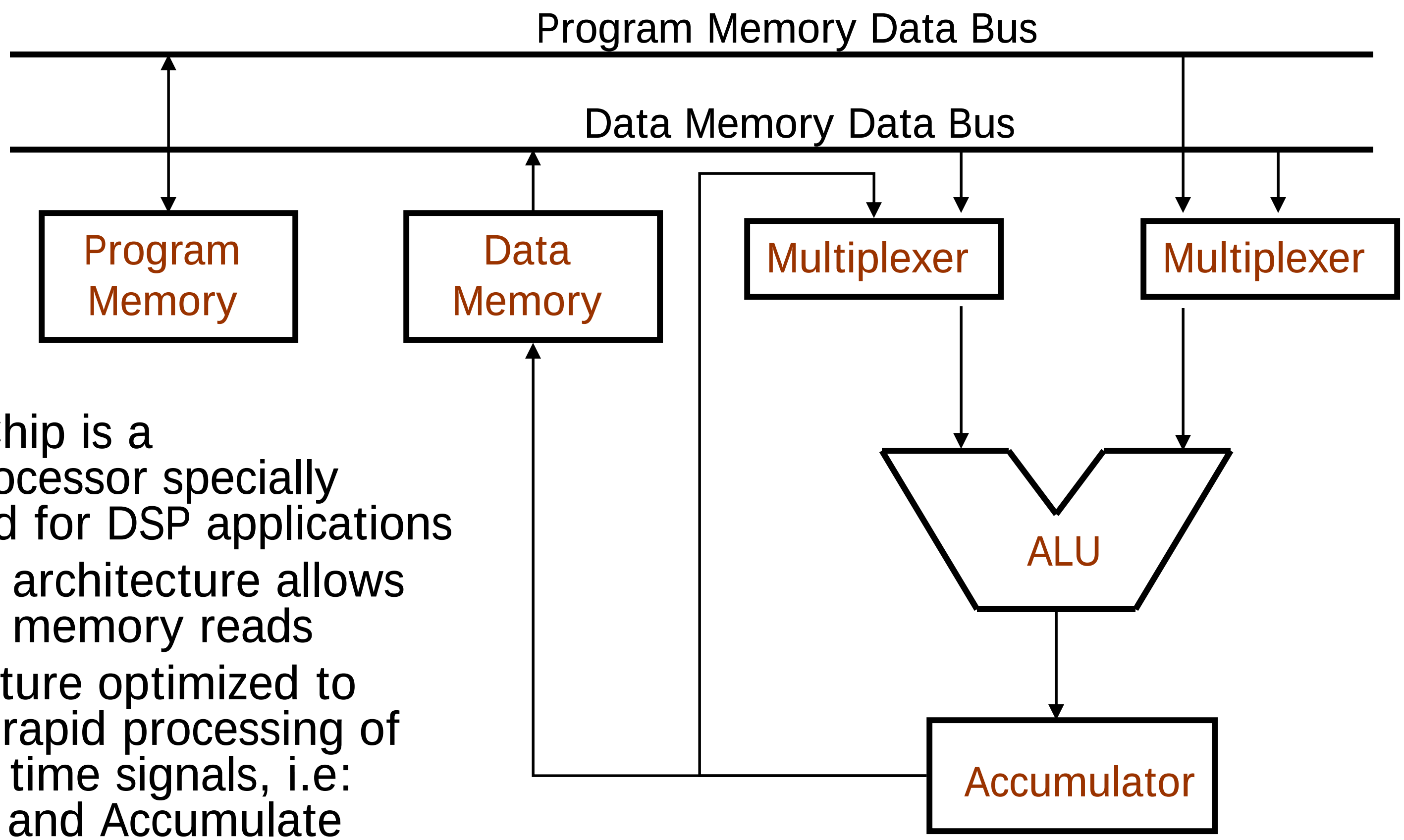
Solution : DSP Architectures

GPP – Data Path Only



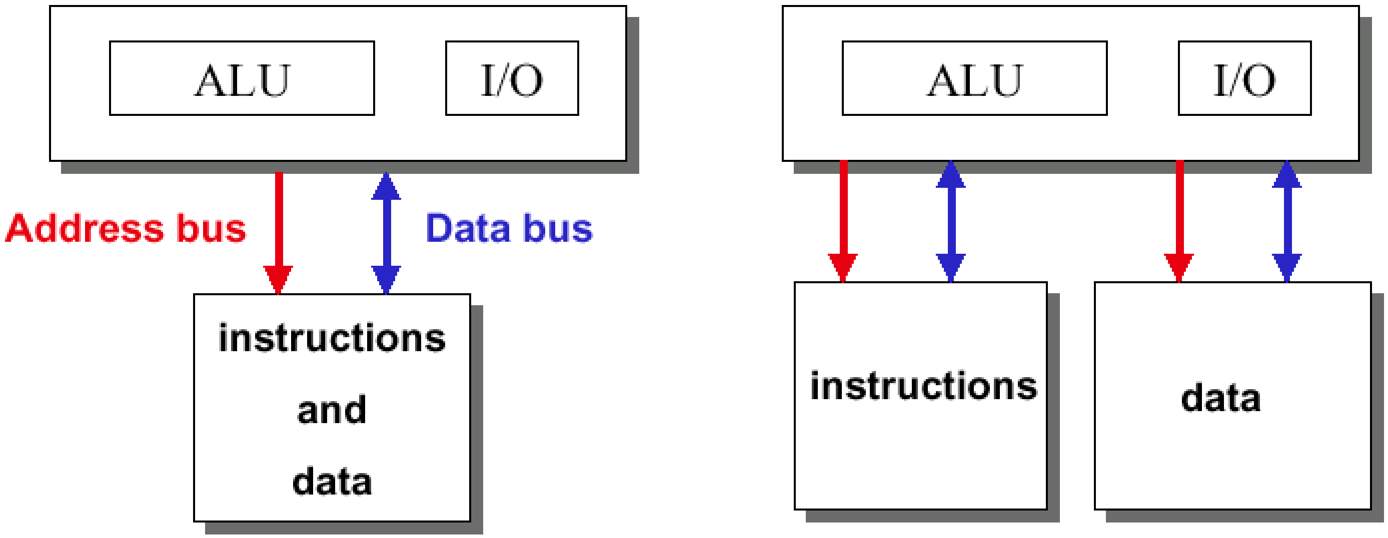
Same memory for program and data

Digital Signal Processors – Data Path Only



- A DSP Chip is a microprocessor specially designed for DSP applications
- Harvard architecture allows multiple memory reads
- Architecture optimized to provide rapid processing of discrete time signals, i.e: Multiply and Accumulate (MAC) in one cycle

Memory structures



Von Neuman architecture
Area efficient but requires higher bus bandwidth because instructions and data must compete for memory.

Harvard architecture was coined to describe machines with separate memories.
Speed efficient: Increased parallelism.

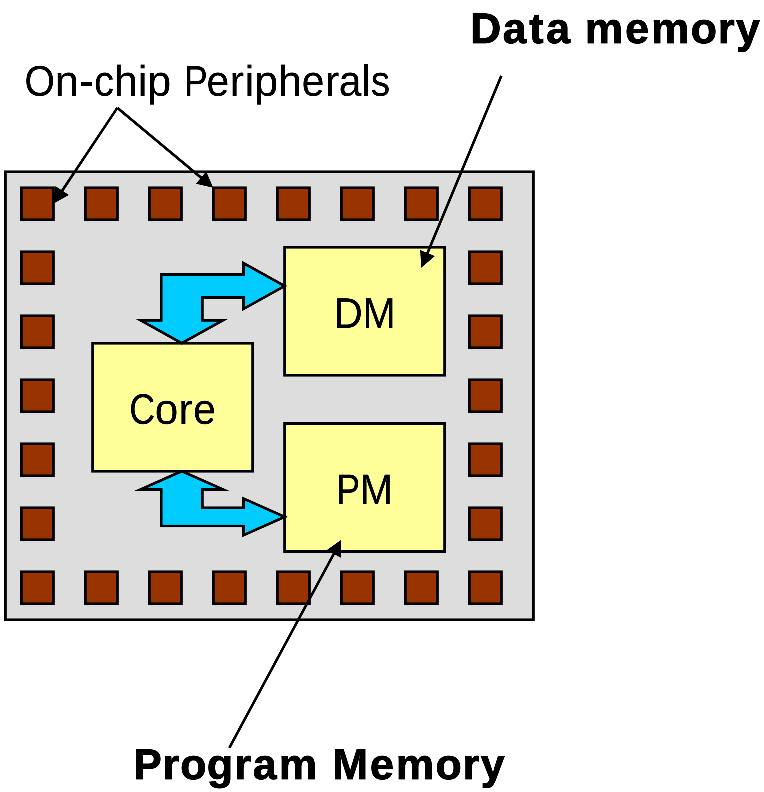
DSP versus GPP

- Multiple parallel units
  - multiply accumulate (possibly several units)
  - address calculation in parallel to processing
  - barrel shifter
- Memory Access
  - special ALU for address calculation
  - Bit reversed addressing
  - circular addressing
- Automatic loops
  - Software looping: writing assembly code to perform branching
  - Hardware looping: dedicated hardware loop counter register
- Hardware support for managing arithmetic computation (in GPP it needs multiple cycles)
  - Shifters
  - Guard bits
  - Saturation

Preventing Overflow!!

Digital Signal Processor (DSP) - Overview

- DSP Core includes:
  - Address buses
  - Data buses
  - Data arithmetic logic unit (ALU)
  - Address generation unit (AGU)
  - Program controller
  - Bit-manipulation unit
  - Enhanced debugging module
- Peripherals on chip
  - Timer
  - serial link
  - communication links
    - DSP to DSP
    - Ethernet
    - ATM
  - host ports
  - input/output pins
- Adaptation for FFT
  - bit reverse addressing
- Special instructions
  - Parallel move support
  - Loop instructions; special hardware instructions (i.e: FIR)



Enhancing DSP Architectures

- More parallelism
  - Increase the number of operations that can be performed in each instruction
    - Adding More Executing units (i.e: Multipliers)
  - Increase the number of instructions that can be issued and executed in every cycle
- Highly specialized hardware in core
- Co-processors
- Multi-Core DSPs

Example: TI OMAP Chip

- Integrates a TMS320C55x™ DSP core with an ARM GPP on a Single Chip
- Targeted for embedded applications
- ARM interfacing peripherals:
  - Bluetooth
  - IrDA
  - Keypad
  - Touch Screen
- C55x to perform DSP algorithms
  - Mobile Messaging
  - Handwriting Recognition
  - Digital Cameras Image processing
- OMAP 2 (released May 2005) Architecture includes a dedicated
  - Image and video accelerator
  - 3D graphics accelerator

Click here to check cell phones and PDAs using TI DSPs and OMAP

Example: TI DaVinci Processors

- Released in Dec 2005.
- Also known as TMS320DM644x series.
- While OMAP targets mainly wireless and handled applications, DaVinci targets home entertainment, surveillance, and other video applications.
- Can perform coding/decoding of standard video codec: MPEG4, H.264.
- Include camera and video interfaces.

What are the alternatives

- Application Specific Integrated Circuits (ASIC)
- Field Programmable Gate Array (FPGA)

ASIC

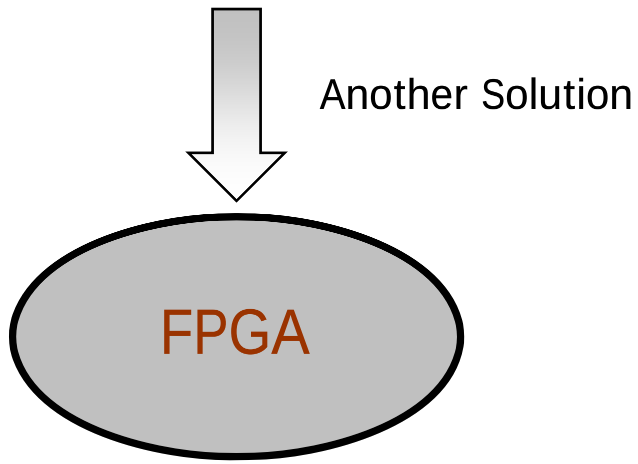
- Uses hard-wired logic with varied architectures according to the application (i.e: hardware-implemented 256-point FFT)

ASIC - Advantages

- Speed
- Reduced Power Consumption

ASIC- Disadvantage

- Large development costs
- Lengthy development cycles
- Inflexibility



What is FPGA

- It is a network of reconfigurable hardware with reconfigurable interconnect controlled by a switching matrix
- Historically used for prototyping
- Recently includes DSP features
  - Major Companies DSP + FPGA: ALTERA & XILINX

FPGA - Advantages

- More Flexible than ASIC
- Huge Performance Gain in Some Applications
- Re-use Hardware for different applications

FPGA - Disadvantages

- Long Development Cycle
- Expensive compared to DSP
- Much higher power consumption compared to DSP
- Slow time to market compared to DSP

Why use DSP?

- Comparison: DSP, FPGA, ASIC (ref: Bill Dally, Stanford University, IEEE ICASSP04 Talk)

DSP

- < 10 MOPS/mW
- ~0.1 GOPS/$
- < 10 GOPS peak performance
- 1 M $ programming cost
- Programmable

ASIC

- 50-200 MOPS/mW
- 2-10 GOPS/$
- Up to 1000 GOPS peak performance
- 10M-15M $ design cost
- Fixed

FPGA

- 2-10 MOPS/mW
- ~1 GOPS/$
- Up to 500 GOPS peak performance
- ~5M $ design cost
- Reconfigurable

- New improved DSPs with more efficiency and parallelism (e.g., multi-core)

What Chip will be used?

- Freescale DSP56858
  - Family: DSP56800E
  - Kit: DSP56858EVM
  - Software: Metrowerks CodeWarrior
    - Metrowerks is a Freescale company in charge of developing the software
  - Applications
    - Telephony
    - Client side IP phone
    - Internet Audio
    - Voice Processing
- TI TMS320C5510
  - Family: TMS320C55xx
  - Kit: TMS320C5510DSK
  - Software: TI Code Composer Studio
  - Applications

Types of DSP

- Low End **Fixed Point**
  - TMS320C2XX, ADSP21XX, DSP56XXX
- High End **Fixed Point**
  - TMS320C55XX, DSP16XXX,
  - ADSP215XX, DSP56800
- Floating Point
  - TMS320C3X, C67XX, ADSP210XX, DSP96000, DSP32XX
- Berkeley Design Tech. Inc. Pocket Guide to DSPs

  http://www.bdti.com/pocket/pocket.htm

Fixed Point Vs Floating Point

- Fixed Point/Floating Point
  - fixed point processor are :
    - cheaper
    - smaller
    - less power consuming
    - Harder to program
      - Watch for errors: truncation, overflow, rounding
    - Limited dynamic range
    - Used in 95% of consumer products
  - floating point processors
    - have larger accuracy
    - are much easier to program
    - can access larger memory
  - It is harder to create an efficient program in C on a fixed point processors than on floating point processors

Fixed Point Vs Floating Point

Texas Instruments

Floating Point

Applications

- Modems
- Digital Subscriber Line (DSL)
- Wireless Basestations
- Central Office Switches
- Private Branch Exchange (PBX)
- Digital Imaging
- 3D Graphics
- Voice over IP

Fixed Point

Applications

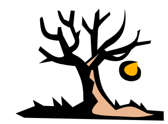
- Portable Products
- 2G, 2.5G and 3G Cell Phones
- Digital Audio Players
- Digital Still Cameras
- Electronic Books
- Voice Recognition
- GPS Receivers
- Headsets
- Biometrics
- Fingerprint Recognition

Motorola Family Tree

Ref: Motorola DSP Selection Guide: http://www.freescale.com/files/shared/doc/selector_guide/SG1004.pdf

Freescale DSP Family Tree [2003]

Floating Point DSP Chips Discontinued!!



TI Tree

56800

DSP56F801
DSP56F802
DSP56F803
DSP56F805
DSP56F807
DSP56F826
DSP56F827

56800E

DSP56852
DSP56853
DSP56854
DSP56855
DSP56857
DSP56858
MC56F8322
MC56F8323
MC56F8345
MC56F8346
MC56F8356
MC56F8357

56300

DSP56301
DSP56303
XC56309
XC56L307
DSP56311
DSP56321
DSPB56362
DSPB56364
DSPB56366
DSPA56367
DSPA56371

MSC8100

MSC8101
MSC8103

56800 DSP Family, 16-bit Fixed Point

Specifications

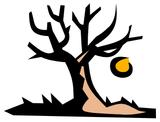
- **Processing capability of up to 35 million instructions per second (MIPS)**
- **Running at 70 MHz**
- **Requires only 2.7–3.6 V of power**

Features

- **Single-instruction cycle 16-bit x 16-bit parallel multiply-accumulator**
- **Two 36-bit accumulators including extension bits**
- **Single-instruction 16-bit barrel shifter**
- **Parallel instruction set with unique DSP addressing modes**
- **Low-power wait and stop modes**
- **Operating frequency down to DC**
- **16-bit Timer Module**
- **Synchronous serial interface module (SSI)**
- **Serial peripheral interface (SPI)**
- **Programmable general-purpose I/O**

Applications

- **Motion Control**
  - ✓ **Smart appliances**
  - ✓ **Environmental controls**
  - ✓ **Instrumentation**
- **Industrial**
  - ✓ **Uninterruptable power supplies**
  - ✓ **Noise cancellation/suppression**
  - ✓ **Temperature control**
  - ✓ **HVAC**
  - ✓ **Inverters and AC-to-DC conversion**
  - ✓ **Lighting**
  - ✓ **Automation**
- **Transportation**
- **Instrumentation**



56800E DSP Family, 16-bit Fixed Point

Specifications

- **Processing capability of up to 120 million instructions per second (MIPS)**
- **Running at 120 MHz**
- **Requires only 2.7–3.6 V of power**

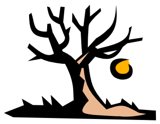
Includes Also the MC56F300 Series which contains on chip Flash memory

Features

- **40K x 16-bit Program SRAM**
- **24K x 16-bit Data SRAM**
- **1K x 16-bit Boot ROM**
- **Access up to 2M words of program memory or 8M data memory**
- **Six (6) independent channels of DMA**
- **Two (2) Enhanced Synchronous Serial Interfaces (ESSI)**
- **Two (2) Serial Communication Interfaces (SCI)**
- **Serial Port Interface (SPI)**
- **8-bit Parallel Host Interface**
- **General Purpose 16-bit Quad Timer**
- **JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging**
- **Computer Operating Properly (COP)/Watchdog Timer**
- **Time-of-Day (TOD)**
- **Up to 47 GPIO**

Applications

- **Telephony**
  - ✓ **Telco interface**
  - ✓ **Codecs**
  - ✓ **LCD and Keypad support**
- **Client-side IP phone**
- **Internet Audio**
  - ✓ **Internet Audio decoding**
  - ✓ **Internet Audio stand-alone player**
- **Voice Processing**



56300 DSP Family, 24-bit Fixed Point

Specifications

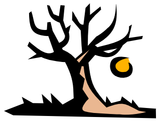
- **Processing capability of up to 480 million instructions per second (MIPS)**
- **Running at 240 MHz**
- **Requires only 1.6–3.3 V of power**

Features

- **Object code compatible with the DSP56000 core with highly parallel instruction set**
- **Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)**
- **Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses**
- **Digital Phase Lock Loop (DPLL) allows change of low-power Divide Factor (DF) without loss of lock**
- **Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)**
- **Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1**
- **Serial Communications Interface (SCI)**
- **Triple timer module**
- **Up to 34 GPIO**

Applications

- **Multimedia**
- **Telecommunciation**
- **Video conferencing**
- **Base transceiver stations**
- **Packet telephony**



MSC8100 Family, 16-bit Fixed Point

Specifications

- **Processing capability of up to 4400 million instructions per second (MIPS)**
- **Running at 300 MHz**
- **Requires only 1.6–3.3 V of power**

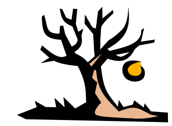
Optimized for networking infrastructure applications

Features

- **Four 250/275 MHz StarCore SC140 DSP extended cores**
- **16 ALUs on a chip deliver up to 4000/4400 MMACS**
- **Performance equivalent to a 1.0/1.1 GHz SC140 Core**
- **Industry's largest on-chip SRAM memory**
- **1436 KB of internal memory**
- **Efficient multi-level memory hierarchy**
- **Dual external industry-standard 60x-compatible buses**
- **9.6 Gbps peak bus throughput**
- **Four independent Time-Division Multiplex (TDM) Interfaces**
- **400 Mbps peak serial data throughput**
- **Accesses various external memories, including SDRAMs, SRAMs, SSRAMs, EPROMs, and Flash**

Applications

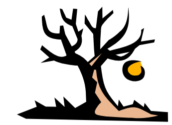
- **2.5G Wireless System**
- **3G Wireless System**
- **IP Telephony**
- **Compression**
- **G.7xx speech coders**



TI Family Tree

Ref: TI DSP Selection Guide

[*http://focus.ti.com/lit/ml/ssdv004m/ssdv004m.pdf*](http://focus.ti.com/lit/ml/ssdv004m/ssdv004m.pdf)

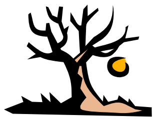


[**Freescale Tree**]()

TI DSP Family Tree [2003]

- C2000
  - C24x: **F2407, F2406, F2403, F2402, F2401, C2406, C2404, C2402, C2401, F243, F241, C242, F240**
  - C28x: **F2810, F2812**
- C3000
  - C3x: **C33, C32, C31, C30**
- C5000
  - C54x: **C5416, C5410, C5409, C5407, C5404, C5402, C5401, C549, C54CST, C54V90**
  - C54x + RISC: **C5470, C5471**
  - C55x: **C5510**, **C5509, C5502, C5501**
  - C55x + RISC: **OMAP5910**
- C6000
  - C62x: **C6211, C6205, C6204, C6203, C6202, C6201**
  - C64x: **C6416, C6415, C6414, C6412, C6411, DM640, DM641, DM642**
  - C67x: **C6713, C6712, C6711, C6701**

TMS320C24x ™ DSP Generation, 16-bit Fixed Point - Control Optimized DSP



Specifications

- Up to 40-MIPS operation
- Three power-down modes
- 3.3-V and 5-V designs

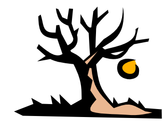
Features

- 375-ns (minimum conversion time) analog-to-digital (A/D) converter
- Dual 10-bit A/D converters
- Up to four 16-bit general-purpose timers
- Watchdog timer module
- Up to 16 PWM channels
- Up to 41 GPIO pins
- Five external interrupts
- Up to 32K words on-chip sectored Flash
- I/O Modules
  - Controller Area Network (CAN) interface module
  - Serial communications inter-face(SCI)
  - Serial peripheral interface (SPI)
- Boot ROM (LF240x and LF240xA devices)

Applications

- Appliances
- Compressors
- Industrial automation
- Uninterruptible power (UPS) systems
- Automotive braking steering systems
- Electric metering
- Printers and copiers
- Hand-held power tools
- Electronic cooling Intelligent sensors
- Tunable lasers
- Consumer goods
- Fuel pumps
- Industrial frequency Remote monitoring
- ID tag readers

TMS320C28x ™ DSP Generation, 16-bit Fixed Point – Control Optimized DSP



Specifications

- 32-bit fixed-point C28x™ DSP core
- 150-MIPS operation
- 1.8-volt core and 3.3-volt peripherals

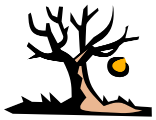
Features

- Ultra-fast 20–40 ns service time to any interrupts
- 32-/64-bit saturation, single-cycle read-modify-write instructions, and 64/32 and 32/32 modulus division
- High-performance ADC
- 32 ×32 single-cycle fixed-point MAC
- Dual 16 ×16 single-cycle fixed-point MACs
- On Chip flash memory
- I/O modules: SPI, SCI, CAN

Applications

- Lighting
- Optical networking (ONET)
- Power supplies
- Industrial automation
- Consumer goods

TMS320C3x ™ DSP Generation, 32 –bit Floating Point – First Generation



Specifications

- Performance up to 150 MFLOPS
- 32 bit Floating point
- Highly-efficient C language engine
- Large address space: 16 Mwords
- Fast memory management with on-chip DMA

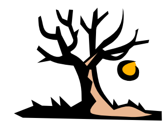
Features

- Parallel multiply and arithmetic/logical operations on integer or floating-point numbers in a single cycle
- Eight extended-precision registers

Applications

- Digital audio
- Laser printers, copiers, scanners
- Bar-code scanners
- Videoconferencing
- Industrial automation and robotics
- Voice/facsimile
- Servo and motor control

TMS320C54x ™ DSP Generation, 16-bit Fixed Point – Power Efficient DSP



Specifications

• 16-bit fixed-point DSPs

• Power dissipation as low as 60 mW for 100 MIPS

• Single- and multi-core products delivering 30–532 MIPS performance

• 1.2-, 1.8-, 2.5-, 3.3- and 5-V versions available

• 6-channel DMA controller per core

Features

• Integrated Viterbi accelerator

• 40-bit adder and two 40-bit accumulators to support parallel instructions

• 40-bit ALU with a dual 16-bit configuration capability for dual one-cycle operations • 17 ×17 multiplier allowing 16-bit signed or unsigned Multiplication

• Four internal buses and dual address generators enable multiple program and data fetches and reduce memory bottleneck

• Single-cycle normalization and exponential encoding

• Eight auxiliary registers and a software stack enable advanced fixed-point DSP C compiler

• Power-down modes for battery powered applications

Applications

• Digital cellular communications

• Personal communications systems (PCS)

• Pagers

• Personal digital assistants

• Digital cordless communications

• Wireless data communications

• Networking

• Computer telephony

• Voice over packet

• Portable Internet audio

• Modems

TMS320C54x ™ DSP + RISC, 16-bit Fixed Point – System Level DSP

Specifications

- Dual CPU processor integrating a TMS320C54x™ DSP core and an ARM7TDMI™ RISC
- 1.8-volt core and 3.3-volt peripherals

Features

TMS320C54x DSP core subsystem

- 100-MIPS operation
- 72 kwords RAM
- Two multi-channel buffered serial ports (McBSPs)
- Direct memory access (DMA) controller
- Phase-locked loop
- External memory interface
- ARM port interface (API)

ARM7TDMI RISC core subsystem

- 47.5-MHz operation
- 16 KByte zero-wait-state SRAM
- Memory interface (SDRAM, SRAM, ROM, Flash)
- Single-port 10/100 Base-T

Ethernet Interface (C5471 DSP only)

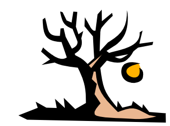
- 36 general-purpose I/O (ARMI/O)
- Two UARTs (one IrDA)
- Serial peripheral interface (SPI)

•I 2 C interface

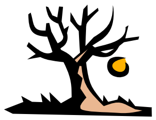
Applications

- wireless data
- Smart pen pads
- Text-to-speech
- Voice recognition
- Vommand control
- Access point controller
- Networked security
- Industrial control and emergency

radio



TMS320C55x ™ DSP Generation, 16-bit Fixed Point – Most Power Efficient DSP



Specifications

• C55x™ DSP core delivers 300 MHz for up to 600-MIPS performance

• 1.6-volt core and 3.3-volt peripherals

Features

• Advanced automatic power management

• Configurable idle domains to extend your battery life

• Shortened debug for faster time-to-market

• 144-MHz/200-MHz clock rate

• 256-KB RAM, 64-KB ROM

• Three McBSPs, I 2 C, watchdog timer, general-purpose timers

• USB 2.0 full-speed (12 Mbps)

•10-bit ADC

•real-time clock (RTC)

Applications

• Feature-rich, miniaturized personal and portable products

• 2G, 2.5G and 3G cell phones and basestations

• Digital audio players

• Digital still cameras

• Electronic books

• Voice recognition

• GPS receivers

• Fingerprint/Pattern recognition

• Wireless modems

• Headsets

• Biometrics

TMS320C55x ™ DSP + RISC, 16-bit Fixed Point – OMAP Processor

Specifications

- Dual CPU processor integrating a TMS320C55x™ DSP core and an ARM925TDMI™ RISC @150 MHz
- 1.8-volt core and 1.8-volt peripherals

Features

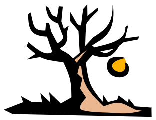
- 150-MHz TI-enhanced ARM925
- 16 KB instruction cache and 8 KB data cache
- Data and instruction MMUs
- 32-bit and 16-bit instruction sets

150-MHz TMS320C55x™ DSP

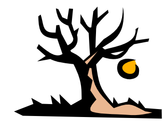
- 12 KW (24 KB) instruction cache
- 80 KW (160 KB) SRAM
- 16 KW (32 KB) ROM
- Two 16-bit memory interfaces for SDRAM and flash
- Nine-channel system DMA controller
- LCD controller
- USB 1.1 host and client
- MMC/SD card interface
- Seven serial ports plus three UARTs, Nine timers, Keyboard interface
- Less than 250 mW at 1.6 V

Applications

- Internet appliances
- Applications processing
- Enhanced gaming
- Webpad
- Point-of-sale
- Medical devices
- Industry-specific PDAs
- Telematics
- Digital media processing
- Military and government cellular



TMS320C62x ™ DSP Generation, 16-bit Fixed Point – High Performance DSP



Specifications

- 16-bit fixed-point DSPs
- Up to 2400 MIPS
- Running at 300 Mhz

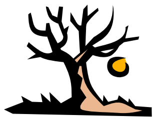
Features

- C6000™ DSP Platform VelociTI™ advanced architecture
- Up to eight 32-bit instructions executed each cycle
- Eight independent, multi-purpose functional units thirty-two 32-bit registers
- Industry's most advanced C compiler and Assembly Optimizer maximize efficiency and performance

Applications

- Pooled modems
- Digital Subscriber Line (xDSL)
- Wireless basestations
- Central office switches
- Private Branch Exchange (PBX)
- Digital imaging
- Call processing
- 3D graphics
- Speech recognition
- Voice over packet

TMS320C67x ™ DSP Generation, 32-bit Floating Point – High Performance DSP



Specifications

- 32-bit loating point DSPs
- Up to 1350 MFLOPS
- Running at 225 Mhz

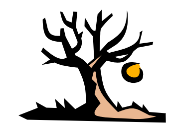
Features

- C6000™ DSP Platform VelociTI™ advanced architecture
- Up to eight 32-bit instructions executed each cycle
- Eight independent, multi-purpose functional units thirty-two 32-bit registers
- Industry's most advanced C compiler and Assembly Optimizer maximize efficiency and performance
- IEEE floating-point format
- Up to 1350 MFLOPS at 225
- Two new multi-channel serial ports (McASP) (C6713 DSP) can support up to stereo channels of I^2S (Inter IC Sound) and compatible with S/PDIF transmit protocol. Note I2S is a protocol for transmitting 2 channels of digital audio over a single serial connection

Applications

- Pooled modems
- Digital Subscriber Line (xDSL)
- Wireless basestations
- Central office switches
- Private Branch Exchange (PBX)
- Digital imaging
- Call processing
- 3D graphics
- Speech recognition
- Voice over packet

TMS320C64x ™ DSP Generation, 16-bit Fixed Point – High Performance DSP



Specifications

- 16-bit fixed point processor TMS320C64x DSP high performance core provides scalable performance of up to 1.1 GHz
- The industry's fastest DSPs with up to 600 MHz (4800 MIPS) performance
- C64x DSPs are software compatible with TI's C62x™ DSPs

Features

- C6000™ DSP Platform VelociTI™ advanced architecture
- Up to eight 32-bit instructions executed each cycle
- Eight independent, multi-purpose functional units thirty-two 32-bit registers
- Industry's most advanced C compiler and Assembly Optimizer maximize efficiency and performance

Applications

- DSL and pooled modems
- Basestation transceivers
- Wireless LAN
- Enterprise PBX
- Multimedia gateway
- Broadband video transcoders
- Streaming video servers and clients
- Highspeed raster image processing (RIP)

TI Families Summary

- C24x and C28x families: low performance 16-bit fixed point used for control purpose
- C54x family: mid-range performance 16-bit fixed point
- C55x family: mid-range performance 16-bit fixed point with reduced power consumption and increased parallelism
- C5000 + RISC microprocessor: used for embedded applications such as cell phone and PDAs
- C62x: high-range performance 16-bit fixed point supporting VLIW architecture
- C64x: very high performance 16-bit fixed point with extension capabilities of C62x with higher clock frequency (>2500 MIPS)
- C3x: first generation low performance 32-bit floating point
- C67xx family: very high performance 32-bit floating point

Software Coding

- Write Code in C
- Compile to create Assembly code
- Assemble the code to create object code and link
- Use simulator to test the speed of the code
- If code is not fast enough - rewrite the C code and test again. If not fast enough yet, write in **Assembly language**

Why use Assembly?

- Most C compilers for DSP chips produce code that does not fully utilize the capabilities of the DSP
  - Data Fetch parallel to execution
  - Parallel execution
- The C code can be 3 to 30 times slower than the best assembly code possible. Especially in the signal processing parts of the code.
- The problem is more acute with fixed-point DSPs

But I don't want to write Assembly

- Have somebody else write assembly for you
  - use libraries
- Rewrite your C code to produce a better assembly code
- Test and profile your code to see which parts of the software take most of the CPU time. Limit Assembly code to subroutines:
  - That the program spends a lot of time in them
  - That benefit from the special functions of DSP such as MACS and parallel execution and fetch.

How to Write a Better C Code

- Use Simple Loops
- Avoid if statements in loops
- Avoid subroutine calls statements in loops
- Use inline subroutines
  - Compiler inserts function directly into the caller's code stream (conceptually similar to what happens with a #define macro)
  - Avoids the subroutine call over head (saving volatile variables)
  - Increases code size
- Avoid division and modulo operations
- Use and (&) and shift when possible
- Use **5%/80%** rule
  - Program in Assembly the 5% of the lines of code of the project that take 80% of the CPU load.
  - Try to change your code to fit existing assembly routines.

DSP Algorithms Vs DSP Processors

- DSP algorithms depict the architecture of DSP processors:
  - DSP algorithms are computationally demanding: more parallel units + hardware accelerator.
  - Numerical accuracy: use of large size accumulators with guard bits + saturation hardware.
  - High memory bandwidth: use of Harvard architecture and with dual access RAM for parallel moves.

DSP Algorithms Vs DSP Processors

- DSP algorithms depict the architecture of DSP processors:
  - Predictable data and memory location access (i.e: Filtering, FFT): use of specialized addressing mode: bit reversed, modulo addressing
  - Math Intensive algorithms: operations conducted using MAC unit(s) -> single instruction cycle.
  - Real time constraints: use of DMA, SRAM memory instead of DRAM.

Evolution of DSP Processors

- Low end conventional DSP processors:
  - Single multiplier or MAC unit and an ALU, one MAC/cycle.
  - Operate at around 20-50 MHz, and provide good DSP performance
  - Low power consumption and memory usage.
- Midrange conventional DSP Processors:
  - Increased clock speeds operating at 100-150 MHz.
  - Include additional hardware, such as a barrel shifter or instruction cache, with a deeper pipeline to improve performance.

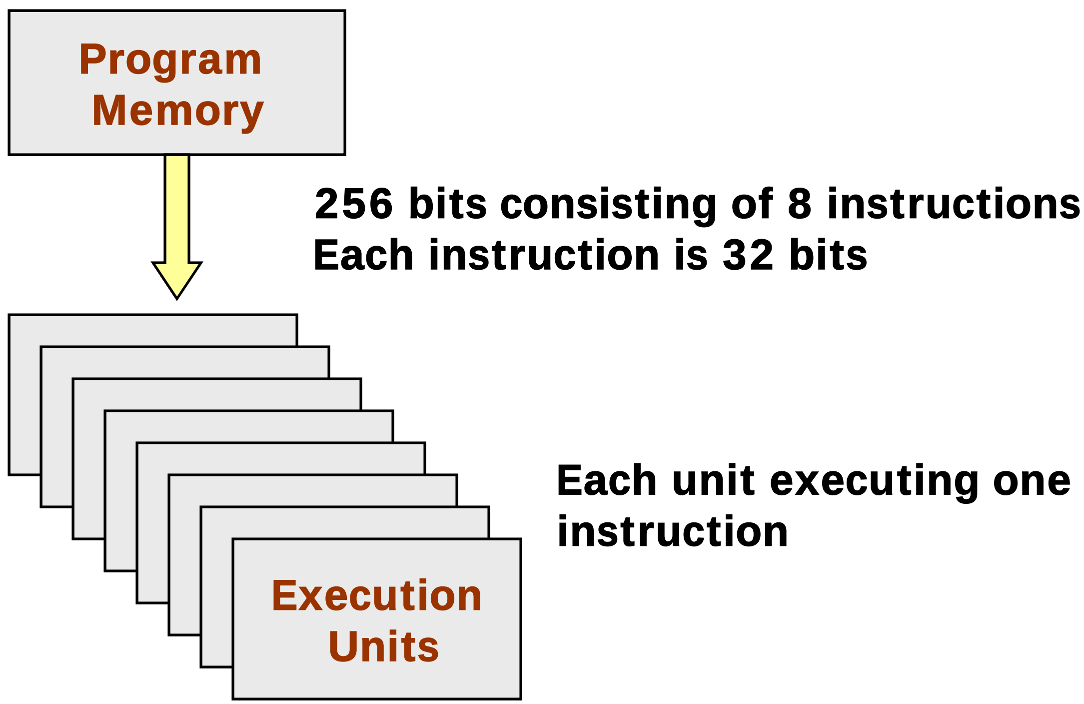
Evolution of DSP Processors

- Enhanced conventional DSP processors:
  - More than one operation /cycle.
  - Extensive use of parallel units.
  - Wider buses for higher data rate.
- Advanced DSP Processors:
  - Use of multi-issue architecture: executing multi instructions in parallel at one time.
  - Higher energy consumption.
  - Use of Single Instruction Multiple Data (SIMD) improving performance by allowing the execution of multiple instances of the same operation on multiple data.
  - Two classes of multi-issue architectures:
    - ✓ Superscalar: dynamic scheduling, difficult to predict the execution time of a routine-> problem for real-time applications, used by high end GPPs.
    - ✓ VLIW (Very Large Instruction Width): static scheduling, instructions are grouped at the time the program is assembled (used by most DSP processors).

Very Large Instruction Width (VLIW)

- VLIW architectures execute multiple instructions/cycle and use simple, regular instruction sets
  - More parallelism, higher performance
  - Better compiler target
- Multiple independent instructions per cycle, packed into single large "instruction word" or "packet“
- Large, uniform register sets
- Wide program and data buses

VLIW – Simplified Architecture Example



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  - Higher energy consumption.
  - Use of Single Instruction Multiple Data (SIMD) improving performance by allowing the execution of multiple instances of the same operation on multiple data.

DSP Processor Selection Criteria

- Wide range of DSP processors are available, which one to select?
- It depends about the application: what is the most important criteria?
  - Speed.
  - Memory bandwidth.
  - Cost.
  - Ease of use of development tools.
  - Packaging options.
  - On-chip integration.
  - Power consumption.

DSP Processor Selection Criteria

- Use of available benchmarks:
  - BDTI kernel benchmarks.
  - BDTI application benchmarks.
- Use a hierarchical approach to pick a processor
  - List your requirements.
  - Start with critical criteria; and prioritize the remaining ones.
  - Trade-offs may be required.