

## **Codes and Standards Model for Wafer Fab Design and Construction**

by Sanjeev Krishnam (Graduate Student, Del E. Webb School of Construction, Arizona State Univ., Tempe 85281-0204), and Allan D. Chasey (Asst. Prof., Del E. Webb School of Construction, Arizona State Univ., Tempe 85281-0204)

### **Abstract**

The Codes and Standards Model is a web-based resource tool which has compiled all the major codes and standards used in the semiconductor industry for the design and construction of a wafer fabrication facility. This resource tool can be used during the programming, design, construction, commissioning, and operations phase of a semiconductor facility. The model provides an executive summary of the code sections, where they could be obtained, and the area of use. It also provides links to various websites to access articles and other material on various cleanroom and semiconductor related issues to improve the design and construction process.